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(54) **MEMORY DEVICES AND RELATED METHOD INCORPORATING DIFFERENT BIASING SCHEMES**

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(57) **ABSTRACT**

Memory devices comprise a plurality of memory cells, each memory cell including a memory element and a selection device. A plurality of first (e.g., row) address lines can be adjacent (e.g., under) a first side of at least some cells of the plurality. A plurality of second (e.g., column) address lines extend across the plurality of row address lines, each column address line being adjacent (e.g., over) a second, opposing side of at least some of the cells. Control circuitry can be configured to selectively apply a read voltage or a write voltage substantially simultaneously to the address lines. Systems including such memory devices and methods of accessing a plurality of cells at least substantially simultaneously are also disclosed.